Attorney's Docket No. 1009683-000476

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
Soichi Kobayashi et al.	Group Art Unit: 2138
Application No.: 10/632,928	Examiner: Saqib Javaid Siddiqui
Filed: August 4, 2003	Appeal No.: _____
For: SEMICONDUCTOR INTEGRATED CIRCUIT CAPABLE OF TESTING WITH SMALL SCALE CIRCUIT CONFIGURATION	

APPEAL BRIEF

Mail Stop APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Date: March 14, 2007

Sir:

This appeal is from the decision of the Examiner dated July 14, 2006 (Paper No. 20060708) in which claims 1, 3-4 and 6-9 were finally rejected. Claims 1, 3-4 and 6-9 are reproduced in the Claims Appendix of this brief.

☐ A check covering the ☐ $ 250 ☐ $ 500 Government fee is filed herewith.

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I. Real Party in Interest

The present application is assigned to Renesas Technology Corp., who is the real party in interest.

II. Related Appeals and Interferences

There are no known currently pending related appeals or interferences in the subject application.

III. Status of Claims

Claims 1, 3-4 and 6-9 remain pending in the subject application and are being appealed.

IV. Status of Amendments

No amendments have been made to claims 1, 3-4 and 6-9 subsequent to the final rejection.

V. Summary of the Claimed Subject Matter

The present invention relates to a semiconductor integrated circuit, and more particularly to a semiconductor integrated circuit having a test function. (Page 1, lines 6-8)

Fig. 1 shows a configuration of a semiconductor integrated circuit in accordance with a first embodiment. Referring to Fig. 1, a semiconductor integrated circuit 100 includes two modules A and B, an external bus I/F8, and a repair code generation circuit 4. Two modules A and B are connected to a common internal address bus and to a common internal data bus and have their operations controlled by their respective chip select signals in a normal operation. (Page 3, lines 19-25)

(Module A)

Module A includes an SRAM (Static Random Access Memory) cell array 51a, a gate circuit 41a, a word driver 5a, an address decoder 6a, a control circuit 7a, a

comparator (CMP) 11a, an error register 12a, an address decoder 13a, a tristate buffer 14a, an NOR circuit 20, an AND circuit 21, an OR circuit 22, and a program circuit 30a. (Page 3, lines 27-31)

SRAM cell array 51a includes memory cells arranged in columns and rows with 33 memory cells in the column direction and 1K memory cells in the row direction. (Page 3, line 32 through page 4, line 1)

Through NOR circuit 20, AND circuit 21, and OR circuit 22, when the memory test mode signal is "1" (asserted) and the 18th bit and the 19th bit of the address signal both are "0", or when chip select signal CS1 is "1" (asserted), the asserted signal is passed from OR circuit 22 to control circuit 7a. (Page 5, lines 18-22)

Control circuit 7a controls writing of data to SRAM cell array 51a and reading of data from SRAM cell array 51a. Control circuit 7a allows a data writing or reading operation to/from SRAM cell array 51a only when the signal from OR circuit 22 is asserted. Therefore, in the memory test mode, data is written into or read from SRAM cell array 51a irrespective of a value of chip select signal CS1. (Page 5, lines 23-28)

Therefore, in module A, where the memory test mode signal is "1" (asserted), the reading or writing operation is performed only when the 18th and 19th bits of the address signal are set to "00", and the reading or writing operation is not performed when the 18th and 19th bits of the address signal are set to "01", "10" or "11". This prevents the same word line from being activated at different times in the memory test mode. (Page 5, line 29 through page 6, line 1)

Module B has a configuration generally similar to module A. It is noted that SRAM cell array 51b of module B includes 4K memory cells in the row direction and 33 memory cells in the column direction. Here, one column is provided for a redundancy circuit. In order to select a memory cell within SRAM cell array 51b, 4K word lines and 33 bit line pairs are provided. (Page 6, lines 16-21)

Module B does not include NOR circuit 20, AND circuit 21, and OR circuit 22, but includes an OR circuit 23. (Page 6, lines 22-23)

In the memory test mode, the memory test mode signal is set to "1" (asserted) in accordance with the external control signal. On the other hand, in the normal mode, chip select signal CS2 is set to "1" (asserted) when module B is selected in

accordance with the external control signal. OR circuit 23 outputs to control circuit 7b a signal to be asserted when the memory test mode signal is "1" (asserted) or when chip select signal CS2 is "1" (asserted). (Page 6, lines 24-30)

Control circuit 7b controls writing of data to SRAM cell array 51b and reading of data from SRAM cell array 51b. Control circuit 7b allows writing or reading of data to or from SRAM cell array 51b only when a signal output from OR circuit 23 is asserted. Therefore, in the memory test mode, data is written into or read from SRAM cell array 51b irrespective of a value of chip select signal CS2. (Page 6, line 31 through page 7, line 3)

The foregoing features are encompassed by applicants' independent claim 3. Claim 3 is directed to the device shown in Figures 1, 7 and 8. In particular, the semiconductor integrated circuit comprises a plurality of modules having word lines different in number. Each module has a control circuit. The control circuit, included in a module that does not have a maximum number of word lines, controls an operation of reading or writing data in a test mode, irrespective of a value of a chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values. Thus, the semiconductor integrated circuit prevents the same word line from being activated at different times in a memory test mode.

VI. Grounds of Rejection to Be Reviewed on Appeal

The issues for review by the Board of Patent Appeals and Interferences are:

1) whether claims 1, 3-4 and 6 were properly rejected under 35 U.S.C. §102(b) as being anticipated by *Kawamata* (U.S. Publication No. 2001/0042231); and

2) whether claims 7-9 were properly rejected under 35 U.S.C. §103 as being unpatentable over *Kawamata* in view of *Urakawa* (U.S. Patent No. 6,324,106).

VII. Argument

A. Rejection of claims 1, 3-4 and 6 under 35 U.S.C. §102(b) over *Kawamata*

Applicants respectfully submit that the prior art does not show, teach or suggest a) a plurality of modules having word lines different in number, b) each of the plurality of modules has a control circuit controlling the operation of reading or writing to or from the memory cells of the module, c) the control circuit of a module that does not have a maximum number of word lines controls reading or writing irrespective of the value of the chip select signal in a test mode, and d) the control circuit in the module that does not have a maximum number of word lines controls reading or writing based upon bits in an address signal which are at prescribed values as claimed in claim 3.

Kawamata appears to disclose in Figure 5, a plurality of fail information memories 110-113 for a main memory array and one fail information memory 20 for redundant cells, each having addresses A0-A21. Thus nothing in *Kawamata* shows, teaches or suggests a plurality of modules having word lines different in number as claimed in claim 3. Rather, *Kawamata* teaches away from the claimed invention since all of the main memory cell arrays 110-113 and redundant cell array 20 contain the same number of address lines. Thus, all cell arrays in *Kawamata* have the same number of word lines, whereas as claimed in claim 3, the modules have word lines different in number.

Applicants respectfully traverse the Examiner's statement in the Advisory Action dated January 26, 2007 that *Kawamata* tests memories with "different word lines." First, applicants respectfully point out that "different word lines" is not claimed in claim 3. What is claimed in claim 3 are modules having word lines different in number. Furthermore, paragraphs [0057] and [0058], of *Kawamata* and in particular [0058], merely disclose that the difference between prior art Figure 4 and prior art Figure 5 is that the memories can be smaller. In other words, Figure 4 of *Kawamata* shows address lines A0-A22 while Figure 5 shows address lines A0-A21. Nothing in *Kawamata* shows, teaches or suggests using a combination of cells from Figure 4 and cells from Figure 5 in the same semiconductor integrated circuit. Rather, all arrays from Figure 4 have the same number of addresses A0-A22 and all arrays in

Figure 5 contain the same number of addresses A0-A21. Thus nothing in *Kawamata* shows, teaches or suggests a plurality of modules having word lines different in number as claimed in claim 3.

Additionally, *Kawamata* merely discloses both channel data bits D0-D3 and a redundant signal are input to the main memories 110-113 and the redundant memory 20. Nothing in *Kawamata* shows, teaches or suggests each of the plurality of modules has a control circuit controlling the operation of reading or writing to or from the memory cells of the module as claimed in claim 3. Rather, *Kawamata* only discloses channel data bits and a redundant signal are input to the main memories 110-113 and redundant memory 20.

Applicants respectfully traverse the Examiner's interpretation of the claim language. The Examiner interprets the claim language "each module has a control circuit" to mean that all modules are linked to one control circuit. Applicants respectfully submit that such a feature is not claimed, is not disclosed in the specification and is not shown in the drawings. The Examiner's interpretation is erroneous. Applicants respectfully submit that claim 3 clearly claims a plurality of modules, each having a control circuit. Applicants respectfully request the Board correctly interprets claim 3.

Furthermore, *Kawamata* merely discloses at paragraph [0057] supplying the fail signal of the channel data bit D0 to a chip select terminal (CSB) in order to indicate whether information should be written into the module. Thus nothing in *Kawamata* shows, teaches or suggests controlling reading or writing irrespective of a value of a chip select signal in a test mode as claimed in claim 3. Rather, the chip select terminal in *Kawamata* is activated when information is to be written into a cell.

Finally, *Kawamata* merely discloses a redundancy signal which indicates testing of the main cell array or redundant cells, and if the redundant cells are to be tested, the write enable terminal is inactivated so that the fail information memory is put in a condition unable to write ([0059]-[0061]). Thus nothing in *Kawamata* shows, teaches or suggests controlling reading or writing based upon values of bits in an address signal which are at prescribed values as claimed in claim 3. Rather, *Kawamata* only discloses controlling reading/writing based upon the redundancy signal.

Claims 1, 4 and 6 stand or fall with claim 3. Since nothing in *Kawamata* shows, teaches or suggests a) a plurality of modules having word lines different in number, b) each module has a control circuit controlling the operation of reading or writing into memory cells of that module, c) controlling the operation of reading or writing irrespective of a chip select value in a test mode, and d) controlling reading or writing in a test mode only when values of prescribed bits in an address signal are prescribed values as claimed in claim 3, applicants respectfully request the Board of Patent Appeals and Interferences reverses the Examiner's rejection of claim 3 under 35 U.S.C. §102(b). In addition, since claims 1, 4 and 6 depend from claim 3, applicants respectfully request the Board of Patent Appeals and Interferences reverses the rejection of these claims under 35 U.S.C. §102(b).

B. Rejection of claims 7-9 under 35 U.S.C. §103 as being unpatentable over *Kawamata* in view of *Urakawa*

Applicants respectfully submit that the dependent claims 7-9 will stand or fall with claim 1. However, applicants respectfully submit that since claim 3 is not anticipated by *Kawamata*, applicants respectfully request the Board of Patent Appeals and Interferences reverses the Examiner's rejection of claims 7-9 under 35 U.S.C. §103.

VIII. Conclusions

For all of the above-stated reasons, applicants respectfully request the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this application since applicants respectfully submit that the rejection of claims 1, 3-4 and 6-9 is in error.

IX. Claims Appendix

See attached Claims Appendix for a copy of the claims involved in the appeal.

X. Evidence Appendix

See attached Evidence Appendix for copies of evidence relied upon by applicants (none).

XI. Related Proceedings Appendix

See attached Related Proceedings Appendix for copies of decisions identified in Section II, supra (none).

Respectfully submitted,

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VIII. CLAIMS APPENDIX

The Appealed Claims

1. The semiconductor integrated circuit according to claim 3 further comprising:

a comparator comparing a value of data read from each memory cell connected to an activated word line with an expected value to be read from said each memory cell, for each column in a test mode; and

an error register accumulatively holding error data based on a comparison result by said comparator, wherein

each bit of said error data indicates said comparison result by said comparator for a corresponding column, and

said each bit takes a first logical value when said comparison result for said corresponding column always indicates equality whichever word line is activated, and takes a second logical value when once said comparison result for said corresponding column indicates difference.

3. A semiconductor integrated circuit comprising:

a plurality of modules having their operations controlled by respective chip select signals,

said each module has a plurality of memory cells; and

said each module has a control circuit controlling an operation of reading or writing data from or into said memory cell,

said plurality of modules receive a common address signal sent through a common internal address bus, where said plurality of modules have word lines different in number,

said control circuit included in a module that does not have a maximum number of word lines controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of said chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values.

4. The semiconductor integrated circuit according to claim 3, wherein said prescribed bits are used in specifying a word line of a module having a maximum number of word lines and are not used in specifying a word line of said module that does not have a maximum number of word lines.

6. The semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a redundancy circuit in a column.

7. The semiconductor integrated circuit according to claim 6, wherein said error register outputs held error data when an address signal indicates a prescribed value,

said semiconductor integrated circuit further comprising a repair code generation circuit receiving said error data for generating a repair code for repairing a defective memory cell array using said redundancy circuit.

8. The semiconductor integrated circuit according to claim 7 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register; and

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector.

9. The semiconductor integrated circuit according to claim 6 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register;

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector; and

a processor controlling an execution of a two-step test, wherein

said processor controls writing of test data into a memory cell and reading of test data from a memory cell without causing said repair control circuit to perform repair in a first step of the test,

generates a repair code corresponding to error data stored in said error register in said first step of the test for storage into said register, and

controls writing of test data into a memory cell and reading of test data from a memory cell while allowing said selector to output the repair code from said register to cause said repair control circuit to perform the repair.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.